Homework 2

Q.1.

Following are three scaling challenges:

1. Tunneling current from a polycrystalline Si gate through, for example, a 1.0nm thick SiO2 gate insulator becomes a principal problem which then followed by sub-threshold drain-to-source leakage current.
2. Increasing source and drain resistance is also becoming a significant issue causing larger transistor latency.
3. static and dynamic power dissipation become major problems limiting the rate of advance of Si technology

Following are technological innovation for scaling:

1. To address the power dissipation problem in multi-core microprocessors, techniques such as power and clock gating of entire cores and adjustment of individual core-clock frequency are among the methods being introduced.
2. Innovation has been the use of high-permittivity (hi-k) gate-dielectric materials such as hafnium oxide (HfOx) and metal-gate electrodes such as TiN.